

MEMORY DEVICE AND METHOD OF  
READING DATA FROM A MEMORY DEVICE

ABSTRACT

The present invention relates to a memory device which enables a greater amount of time to read data into a buffer. In particular, a memory device according to one aspect of the present invention comprises a delay-locked loop circuit having a plurality of delay elements and a synchronization circuit coupled to the delay-locked loop circuit. The synchronization circuit also receives a synchronization enable signal and outputs a plurality of enable signals, including an enable signal coupled to an output circuit. Because the enable signal coupled to the output circuit is synchronized with the read signal, it is possible to provide more time to read data into the buffer. According to another aspect of the present invention, a method of reading data from a memory device couples a synchronization enable signal to a synchronization circuit. An external clock signal is also coupled to a delay-locked loop circuit. A read signal is generated based upon a synchronization enable signal and a delayed clock signal of the external clock signal. An output enable is also generated based upon the synchronization enable signal and a delayed clock signal of the external clock signal. Because the output signal is synchronized to the read signal, more time is allowed for the sense function.